ensoniq®

SOUNDSCAPE™
BY ENSONIQ

# ES 5706 "ODIE"

## ENSONIQ Soundscape Multimedia PC Host Interface

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# SECTION 1 -INTRODUCTION AND SPECIFICATIONS

## 1.1 INTRODUCTION

The Soundscape™ multimedia audio board is a full Microsoft Level I-compatible audio subsystem based on the ENSONIQ OTTO digital oscillator chip, the Sequoia Development Group ODIE support gate array and the Sequoia Mockingbird-OTTO firmware. OTTO provides up to thirty-two voices of CD-quality 16-bit digitally synthesized sounds at sample rates ranging from a few kHz to well beyond 44 kHz. With ODIE, OTTOs companion gate array, and the Mockingbird-OTTO synthesizer firmware, the Soundscape board exceeds all requirements of the Level I specification.

By careful design and exploitation of the unique combination of features found in OTTO, Soundscape provides very high performance, and a high degree of flexibility in configuration while maintaining a low production cost and low parts count. In fact, Soundscape actually has a lower production cost than some existing Level I audio boards based on the Yamaha YM3812 and OPL-III FM synthesizers.

To maintain maximum compatibility with existing software, the PC interface of Soundscape exactly emulates a Roland MPU-401 MIDI interface, including the "intelligent" mode. With the addition of a Yamaha YM-3812 2-operator FM synthesizer or OPL-III 4-operator FM synthesizer the Soundscape provides an exact emulation of the Creative Labs SoundBlaster, including the DSP interface for voice and MIDI, thus providing 100% compatibility with existing game software.

## 1.2 SPECIFICATIONS

**SYNTHESIZER SECTION:**

| | |
|---|---|
| Architecture: | Digital Wavetable Synthesizer |
| Voices: | Up To 32 |
| Polyphony: | Up To 32 Notes |
| Sample Memory: | Up To 8 Mwords of ROM/SRAM/DRAM |
| D/A Converter: | 16-Bit Linear Serial |
| Maximum Playback Rate: | 44.1 kHz |
| Level And Panning Controls: | Separate 12-Bit L&R Controls For Each Voice |
| Filters: | Separate Configurable 4-Pole Digital Filter For Each Voice |
| Envelopes: | Hardware Envelopes For Amplitude and Filters |
| Effects: | Optional DSP Multiple Effects Processor |
| Firmware: | Sequoia Mockingbird-OTTO |

**FM SYNTHESIZER:**

| | |
|---|---|
| Synthesizer: | Yamaha YM-3812 2-Operator FM or OPL-III 4-Operator FM |
| Number of Voices: | 11 (YM3812) or 20 (OPL-III) |
| Base Port Address: | 228H, 238H or 248H, and/or 388H |

**PCM PLAYBACK SECTION:**

| | |
|---|---|
| Capability: | Simultaneous Playback Of Two Mono Or Stereo Streams |
| D/A Converter: | 16-Bit Linear Serial |
| Maximum Playback Rate: | 44.1 kHz |
| Level And Panning Controls: | Separate 12-Bit L&R Controls For Each Channel |
| Filters: | Separate Configurable 4-Pole Digital Filter For Each Channel |
| Data Formats: | 8-,12- or 16-Bit Signed Or Unsigned, 8-Bit -Law Compressed. All Formats Either Mono Or Interleaved Stereo |

**DIGITAL RECORDING SECTION:**

| | |
|---|---|
| Capability: | Mono or Interleaved Stereo Recording |
| A/D Converter: | 16-Bit Linear Serial Delta-Sigma Converter |
| Available Sampling Rates: | 44.1, 22.05, 11.025 kHz +/-0.1% |
| Source Selection: | Any Source(s) Via Separate Stereo Record Mixer |
| Level Control: | Individual Software Controls For Each Source |
| Level Control Range: | +30 To 0 dB On Microphone Input<br>0 To -38 dB On All Other Sources |
| Anti-Aliasing Filter: | Digital Decimation Filter |
| Data Formats: | 8-, 12- or 16-Bit Signed Or Unsigned, or 8-Bit -Law Compressed. All Formats Either Mono Or Interleaved Stereo |

**AUDIO MIXING SECTION:**

| | |
|---|---|
| Input Sources: | Synthesizer Output, FM Synthesizer Output, PCM Output, Internal Line Input (CD), External Line Input, MIC Input |
| Output Configuration: | Line Level To 3.5mm Mini-Phone Jack (HeadPhone or Speaker Power Amplifier Optional) |
| Output Level: | Approx. 4V p-p Maximum |
| Level Control: | 12-Bit For Synthesizer & PCM, 5-Bit For All Others |
| Level Control Range: | +0 To -96 dB For Synthesizer & PCM<br>+0 To -34 dB For All Others |
| Frequency Response: | 20-20,000 Hz +/- 1 dB All Inputs |
| Distortion: | < 0.5% All Inputs |
| Signal/Noise Ratio: | > 80 dB All Inputs |

**HOST INTERFACE:**

| | |
|---|---|
| Configuration: | Emulation of MPU-401 Or 68B50 UART-Based MIDI Interface |
| Number of Ports: | 2 |
| Base Port Address: | Software Selectable from 320H, 330H, 340H, 350H |
| Interrupt Usage: | 1, 2, or 3 Software Selectable From 4 |
| DMA Usage: | 1, 2, or 3 Channels, Software Selectable From 6 |
| CD-ROM Interface: | I/O Decode, Bus Buffering and Software DMA and Interrupt Selections Provided For AT-Bus/SCSI Controller |

**MIDI INTERFACE:**

| | |
|---|---|
| Number of Ports: | 1 |
| Connections: | 1 IN, 2 OUT, 1 THRU (with optional expander) |
| MIDI Clock: | 12-Bit, 1 MHz Counter With Synchronized Tempo Updates |
| Software Features: | MIDI Split, Merge And Time-Stamp |

**JOYSTICK INTERFACE:**

| | |
|---|---|
| Configuration: | Standard IBM Compatible Analog Joystick Interface |
| Number of Joysticks: | 2 (4 Axes, 4 Buttons) |

**ON-BOARD PROCESSOR:**

| | |
|---|---|
| Processor: | 8 MHz Motorola 68EC000 |
| Dedicated ROM: | None, All Operating Code Downloaded From Host PC |
| Dedicated RAM: | None, All RAM Is Shared With OTTO Sound Memory |

## SECTION 2 - HOST PC INTERFACE FUNCTIONAL DESCRIPTION

### 2.1 HOST PC INTERFACE OVERVIEW

Refer to Figure 1, Host PC Interface Block Diagram, at the end of this section for the following discussions. The host PC interface consists of a group of 6 to 40 I/O ports. The first two of these ports access an emulation of one of two standard Musical Instrument Digital Interface (MIDI) interfaces: a 68B50-based UART, or a Roland MPU-401, both of which are widely supported by available MIDI software. The next two ports provide a second interface identical in functionality to the emulated MIDI port. This port is generally used for communicating command and status information to the On-Board Processor (OBP), but can also be used to provide emulation of a dual-port MIDI interface. In this configuration, one port could be used to drive the on-board synthesizer, while the second is used to drive an external synthesizer. The next two host interface ports consist of a data port, and an address port, used to select which of the internal registers will be accessed next through the data port. Through this interface, the host CPU can communicate with the on-board processor as well as some of ODIE's internal control and status registers. This architecture allows future expansion of the host register set without requiring a larger block of host I/O addresses, or loss of upward/downward compatibility. Address decoding, data bus buffering, and software selectable IRQ and DMA channel selection are provided for addition of an AT-bus or SCSI controller. The CD-ROM interface can be decoded for 2, 8, 16 or 32 consecutive port addresses.

In addition to the above I/O ports, the host interface uses one or two interrupt levels, and one or two DMA channels. The CD-ROM interface may also use a single interrupt level and DMA channel. Interrupt levels are software selectable from four choices (normally IRQ 2, 7, 12 & 15), while DMA channels are software selectable from six choices (normally 0, 1, 3, 5, 6, & 7). The interrupt and DMA control lines are tri-state-able so that the interrupt and DMA channels can be shared by other "well-behaved" peripherals. In particular, this architecture allows multiple Soundscape boards to be operated in a single PC, sharing the same interrupt and DMA channels. All communications with the host PC are either interrupt- or DMA-driven. In addition, the polarities and protocols for all interrupt and DMA signals are configurable to support a wide variety of host bus interfaces. It would be a simple matter, for example, to adapt the Soundscape design to a Macintosh, Amiga or any other popular computer.

All host interface logic is contained inside ODIE, except for a pair of 74LS245 data bus buffers and a few control and address line buffers. The base address decode for the board is jumper selectable to 320H, 330H, 340H, or 350H.

All I/O operations are performed without incurring wait states, and all data transfers are buffered by ODIE, to virtually eliminate any potential source of incompatibility related to I/O channel timing. All host read data is driven by ODIE, through the 74LS245 data bus buffers, and all write data is latched in ODIE on the rising edge of IOW*, thus making all I/O operations virtually oblivious to I/O bus speed in any machine which is even remotely IBM compatible.

### 2.2 HOST I/O ADDRESS DECODER

The host PC I/O address decoding logic allows the base port address of the Soundscape to be set to 320H, 330H, 340H or 350H. Host address bits 0-2 are decoded to select the specific register to be accessed as indicated in the following table:

| | |
|---|---|
| BASE+0 | MIDI Emulation Control Register |
| BASE+1 | MIDI Emulation Data Register |
| BASE+2 | HOST Interface Control Register |
| BASE+3 | HOST Interface Data Register |
| BASE+4 | ODIE Internal Address Register |
| BASE+5 | ODIE Internal Data Register |

## 2.3 HOST INTERRUPT INTERFACE

The host interrupt level (IRQ) used by ODIE is selectable under software control. Any of four IRQ's can be made software selectable. Generally IRQs 2, 7, 10, 11, 12 and 15 are available. The current default selection is IRQs 2, 7, 12 & 15. ODIE is capable of generating interrupts on any of the following conditions, each of which is separately maskable:

MIDI Emulation RxRDY
MIDI Emulation TxRDY
HOST Interface RxRDY
HOST Interface TxRDY
DMA Terminal Count Reached
MIDI Clock

In addition to the individual interrupt enables, there is also a master enable to completely disable all interrupts at once.

The IRQ lines may be configured to operate in a "sharable" fashion, being tri-stated when not in use, so other boards may share the same interrupt channel if required. In addition, each interrupt is individually configurable as active high, active low or edge triggered, for maximum flexibility, and to permit easy integration of the Soundscape into non-IBM systems.

## 2.4 HOST DMA INTERFACE

The specific DMA channel(s) to be used by the board are software selectable. Any 3 of 6 DMA channels are software selectable. The current selection is channels 0, 1, 3, 4, 5, & 6. In general, an 8-bit DMA channel would used for all 8-bit DMA transfers, and a 16-bit channel would be used for all 12- and 16-bit transfers. To support operation in XT-class machines, ODIE supports 12- and 16-bit transfers over 8-bit DMA channels. ODIE does not, however, support 8-bit transfers over 16-bit DMA channels. ODIE also allows data to be input in one format, and output in a different format, so that, for example, an 8-bit -Law compressed PCM file can be created from a 16-bit signed PCM file by transferring the data to ODIE in 16-bit signed format, and sending it back to the host in compressed format. Using both 8- and 16-bit DMA channels optimizes DMA throughput, and minimizes host CPU overhead.

Since the OTTO memory architecture only allows external access to the sample DRAM on alternate cycles, burst DMA mode is not supported. Instead, single cycle transfers are made, and host transfers are interleaved with OTTO accesses, with all data being buffered by ODIE. The DMA interface is implemented in a "sharable" fashion, with the DRQ line(s) being tri-stated when not in use, so other boards may share the same DMA channel(s) if required. The DRQ and DACK polarities are also programmable for maximum flexibility.

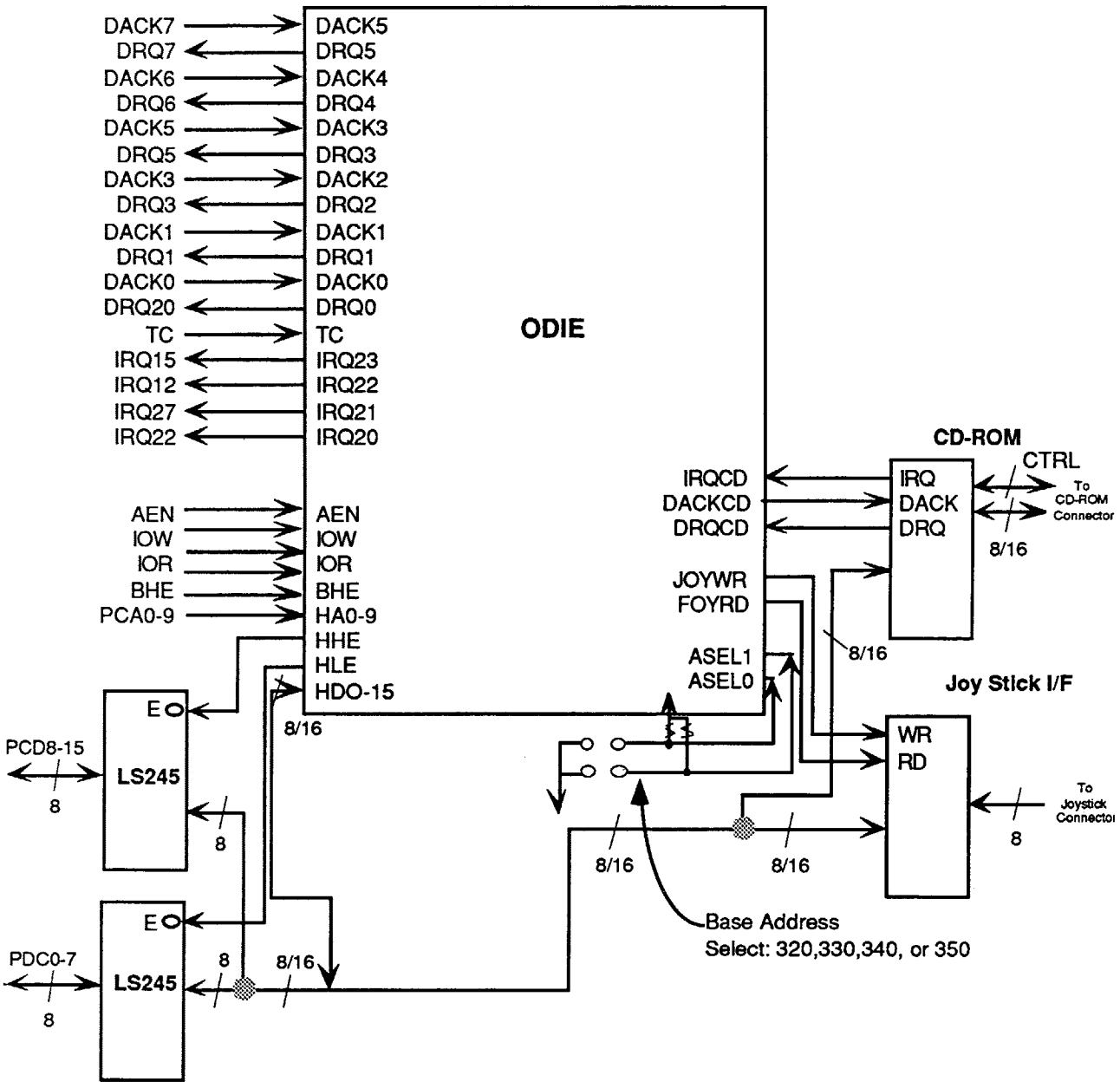


**Figure 1 - Host PC Interface Block Diagram**

## SECTION 3 - ON-BOARD PROCESSOR INTERFACE FUNCTIONAL DESCRIPTION

### 3.1 ON-BOARD PROCESSOR INTERFACE OVERVIEW

Refer to Figure 2, On-Board Processor Interface Block diagram, at the end of this section for the following discussion. The 68EC000 on-board processor (OBP) interface provides all required I/O and memory decoding, DTACK generation, data buffers and latches, and all required system timing and control signals. All of this interface logic is contained within ODIE, along with all of the required peripherals such as the UART for the MIDI interface, the MIDI clock timer, and an interrupt timer. In fact, the only LSIs are the CPU itself, and ODIE. There are no dedicated ROMs for the OBP, as all operating code is downloaded into the on-board DRAM/SRAM via DMA prior to releasing the OBP from reset. A completely ROM-based system can be easily built, however.

### 3.2 ON-BOARD PROCESSOR ADDRESS DECODE

The 16 Mbyte OBP memory space is divided by ODIE into four segments of 4 Mbytes each by decoding the 2 highest address bits. The segments are mapped as follows:

| | | |
|---|---|---|
| Segment 0 | 000000-3FFFFFH | Memory Device 0 (RAM) |
| Segment 1 | 400000-7FFFFFH | Selectable Memory Bank |
| Segment 2 | 800000-9FFFFFH | OTTO Internal Registers |
| | A00000-BFFFFFH | ODIE Internal Registers |
| Segment 3 | C00000-FFFFFFH | Selectable Memory Device |

Segment 0 always maps to memory device 0, which will almost always be either DRAM or SRAM. This is required to support PCM playback. Segment 1 can be mapped to any of the four 4Mbyte banks of OTTO memory space. Segment 2 accesses OTTO and ODIE internal registers. Segment 3 maps to a selectable memory device, which would usually be device 0. This is done to allow the 68000 "short" addressing mode to be used, which not only reduces the code size, but also improves performance.

### 3.3 ON-BOARD PROCESSOR OTTO INTERFACE

OTTO is operated in "slave" mode, allowing ODIE to control all memory accesses. ODIE generates separate CAS*/CS* signals for up to 4 memory devices, each of which can be either SRAM/ROM or DRAM, as well as two WE* signals to allow the OBP byte-access to sound memory. For ROM/SRAM banks, RAS* is used to drive the OE* pins of all memory devices. The memory decoding logic supports any combination of up to 4 DRAMs/SRAMs/ROMs. DRAM configurations from as little as 64Kx8 up to the maximum 8Mx16 can be supported with no additional external logic. The type and configuration of memory actually installed can be determined automatically by the OBP during initialization.

The OBP communicates with the OTTO registers through the OTTO host bus with ODIE generating the required request signal (CSB) to the OTTO.

## 3.4 ON-BOARD PROCESSOR INTERRUPT INTERFACE

All interrupts to the OBP are processed by ODIE. ODIE can generate separately vectored interrupts on the following conditions, listed in order of decreasing priority:

| INTERRUPT SOURCE | VECTOR NUMBER | PRIORITY LEVEL |
|---|---|---|
| MIDI Interface RxRDY/TxRDY | 47H | 6 |
| OTTO Interrupt | 46H | 5 |
| HOST Interface RxRDY/TxRDY | 45H | 4 |
| MIDI Emulation RxRDY/TxRDY | 44H | 4 |
| Interrupt Timer | 43H | 3 |
| DMA A Or B Complete | 42H | 2 |
| MIDI Clock | 41H | 1 |
| SMPTE/MIDI RxRDY | 40H | 1 |

Each interrupt has a separate enable, and a master interrupt enable is also provided.

## 3.5 ON-BOARD PROCESSOR DMA INTERFACE

The DMA control logic, which is completely contained within ODIE, consists of two independent DMA controllers. Several different DMA modes are supported to allow DMA from host to RAM (for loading samples and PCM data), and DMA from RAM to host (primarily for A/D recording). All modes are capable of transferring 8-, 12- or 16-bit data, as appropriate. In addition, there are sub-modes available which largely automate PCM and A/D data transfers. In fact, continuous A/D recording is possible with no assistance from the OBP, once the initial transfer is started. Each of these modes is discussed in more detail in the following sections.

The host DMA channel to be used is programmed by the host CPU before each transfer begins, in order to make it possible to use both 8-bit and 16-bit DMA channels. All operations may be carried out over 8- or 16-bit DMA channels, with the exception of 8-bit DMA over a 16-bit DMA channel, which is not supported.

## 3.6 HOST-TO-RAM DMA OPERATIONS

Host-to-RAM DMA is used both for loading samples and parameters into the sample DRAM, as well as for loading PCM data into buffers in the RAM.

For sample loads, a 16-bit DMA channel is generally used, and transfers start at the address programmed by the OBP into the DMA address register, and end when terminal count is reached. Terminal count can generate an interrupt to the OBP and/or the host CPU.

For PCM data transfers, there are several different options as to how the transfer takes place, since 8-, 12- and 16-bit data must be handled, as well as both mono and interleaved stereo data. Also, the timing of transfers has to be coordinated by the OBP to ensure a buffer is not written to while it is being played.

All PCM transfers take place into circular buffers 4K samples in length. For a mono PCM playback, there is one buffer, while for stereo PCM playback there are two buffers, one for each channel. These buffers MUST be located on consecutive 4K sample boundaries in the sample

DRAM. Each 4K buffer is actually treated as two consecutive 2K buffers. Before playback starts, the entire 4K is pre-loaded. The OTTO is then programmed by the OBP to play a 4K forward loop, and interrupt on end of loop. The OBP calculates the time required to play the first 2K samples, and when that time has elapsed, triggers the DMA to refill the first 2K of the buffer. When the OBP receives the loop end interrupt from OTTO, it triggers the DMA to refill the second half of the buffer. This process continues until PCM playback is stopped.

In order to save the OBP from having to constantly update the DMA address register, and to reduce the DMA overhead on the host CPU, the DMA address counter is able to automatically stop itself after 2K transfers, and automatically reset the address to the start of the buffer after 4K transfers. In this way, the OBP need only tell the DMA hardware when to start the next transfer. The host DMA can also be programmed for a large block size, and the DMA can proceed at it's own pace, not requiring any processor intervention to know when to stop.

If stereo PCM data is being transferred, the process is very similar to that described above, except two consecutive 4K buffers are allocated, and the DMA hardware automatically de-interleaves the data into two separate buffers. Each transfer terminates when 2K samples have been transferred into each buffer (4K samples total). In this way, stereo PCM can be handled with no additional overhead on the OBP.

For 8- and 12-bit PCM transfers, the procedures are exactly as described above, except ODIE always forces the low byte or low nibble of each word to zeroes. Since OTTO expects PCM data to be in signed format, and the Level I standard specifies unsigned format for 8-bit PCM data, ODIE provides the option of unsigned-to-signed conversion of the data on-the-fly.

## 3.7 RAM-TO-HOST DMA OPERATIONS

RAM-to-host DMA is used primarily for transferring sampled (A/D) data to the host. A/D data is buffered in RAM in essentially the same manner as described above for PCM data. However, since ODIE controls the timing of A/D transfers, it is not necessary for the OBP to trigger the DMA. A DMA transfer is automatically initiated as soon as a buffer is half full (2K samples stored).

As a safety precaution, a status flag is set, and can be read by the OBP, if the A/D buffer overflows. This allows the OBP to notify the host CPU that the sampled data may be corrupt.

## 3.8 ON-BOARD PROCESSOR OPERATING CODE DOWNLOAD

In order to allow the OBP to be ROMless, ODIE allows the host to DMA data directly into the RAM while the OBP is inhibited. As explained above, during a normal host-to-RAM DMA, ODIE generates RAM addresses, and all required RAM control signals. By providing a means for ODIE to initiate DRAM refresh without CPU support, the existing DMA logic can be used to load the OBP code into RAM or DRAM. This is accomplished by a control bit within ODIE which forces all OTTO RAM accesses (which take place when the OTTO E clock is high) to be CAS before RAS refresh cycles. Once the OBP has initialized the OTTO to perform normal refresh, this mode is disabled.

## 3.9 SOUND MEMORY INTERFACE

ODIE directly supports up to four memory devices, each of which may be static or dynamic, and each of which may range in size from 64K to 4M. ODIE provides properly latched and/or multiplexed addresses, and CAS*/CS* for all devices. To support this flexibility, three address busses, and five CAS*/CS* lines are provided. The address connections for dynamic memory devices are as follows:

| ODIE Signal | 64Kb Device | 256Kb Device | 1Mb Device | 4Mb Device |
|---|---|---|---|---|
| XA0 | A0/A8 | A0/A17 | A0/A19 | A0/A19 |
| XA1 | A1/A9 | A1/A9 | A1/A18 | A1/A18 |
| XA2 | A2/A10 | A2/A10 | A2/A10 | A2/A20 |
| XA3 | A3/A11 | A3/A11 | A3/A11 | A3/A11 |
| XA4 | A4/A12 | A4/A12 | A4/A12 | A4/A12 |
| XA5 | A5/A13 | A5/A13 | A5/A13 | A5/A13 |
| XA6 | A6/A14 | A6/A14 | A6/A14 | A6/A14 |
| XA7 | A7/A15 | A7/A15 | A7/A15 | A7/A15 |
| XA8 | --- | A8/A16 | A8/A16 | A8/A16 |
| XA9 | --- | --- | A9/A17 | A9/A17 |
| XA10 | --- | --- | --- | A10/A21 |

The address connections for static memory devices are as follows:

| ODIE Signal | ROM or SRAM |
|---|---|
| OA0 | A0 |
| OA1 | A1 |
| OA2 | A2 |
| OA3 | A3 |
| OA4 | A4 |
| LA5 | A5 |
| LA6 | A6 |
| LA7 | A7 |
| LA8 | A8 |
| LA9 | A9 |
| XA0 | A19 |
| XA1 | A18 |
| XA2 | A20 |
| XA3 | A11 |
| XA4 | A12 |
| XA5 | A13 |
| XA6 | A14 |
| XA7 | A15 |
| XA8 | A16 |
| XA9 | A17 |
| XA10 | A10 |
| OA21 | A21 |
| OA22 | A22 |

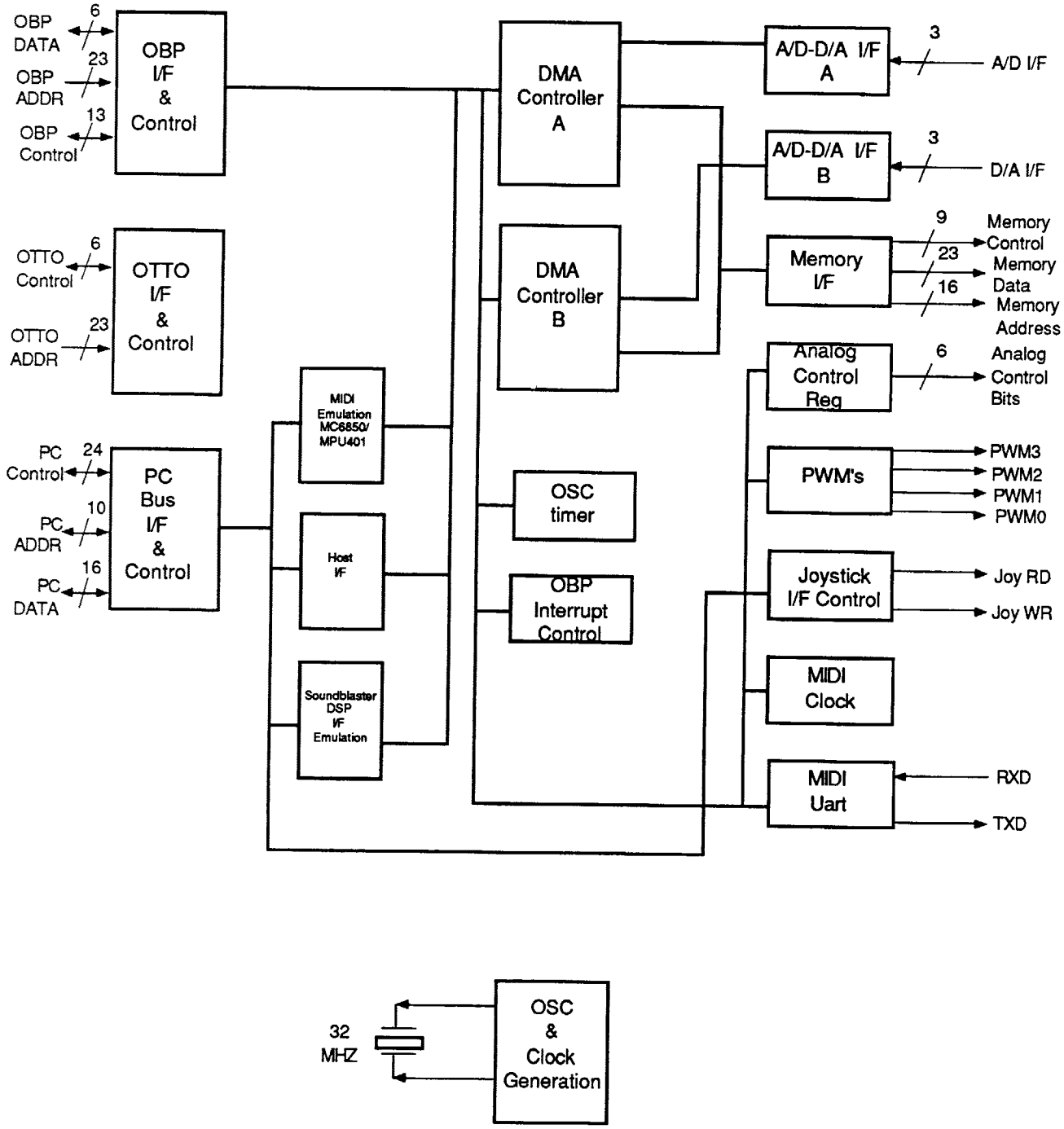


**Figure 2 - On-Board Processor Interface Block Diagram**

# SECTION 4 - ANALOG SECTION FUNCTIONAL DESCRIPTION

## 4.1 - ANALOG SECTION OVERVIEW

Refer to Figure 3, Analog Section Block Diagram, at the end of this section for the following discussion. The analog section of the Soundscape consists of three major sections: i) the OTTO output anti-aliasing filters, ii) the mixer, and iii) the input anti-aliasing filters and A/D converter.

## 4.2 - D/A CONVERTER AND OUTPUT ANTI-ALIASING FILTERS

The serial output of OTTO will be directly connected to a single CD-style 16-bit serial linear delta-sigma stereo D/A converter. Currently, the Philips TDA1545A is used. This is a low-cost, medium-performance "continuous calibration" D/A. The analog current outputs from this converter are directly connected to current-to-voltage converters and 4-pole analog low-pass active anti-aliasing filters. The current-to-voltage converters and filters are implemented using low-cost, low-noise operational amplifiers and 10%-stable (Z5U or C0G) ceramic capacitors. The outputs of the anti-aliasing filters connect directly to an input channel of the audio mixer.

## 4.3 - AUDIO MIXER

The audio mixer section provides mixing and level control of signals originating from the synthesizer, PCM playback, internal (CD) audio, external line-level source, and the FM synthesizer. Level control for the internal and external line sources is achieved by use of the National Semiconductor LMC835 7-band stereo graphics equalizer IC used in a unique mixer mode which provides effectively two separate 5-in stereo mixers. In this configuration, one mixer is used for controlling the line output mix, while the other provides the record mix. A control range of approximately 34dB is provided.

The mixer summing amplifier is an NE5532, gain-scaled to provide a maximum output of approximately 4V p-p, with sufficient output capability to drive high-impedance Walkman-style headphones to reasonable listening levels.

## 4.4 - A/D CONVERTER AND INPUT ANTI-ALIASING FILTERS

The A/D converter section is implemented using the Sony CXD2555Q CoDec, which provides a 16-bit Delta-Sigma A/D with digital filters. The input source is a record mixer descibed above. The microphone inputs are buffered by single-stage operational amplifier preamplifiers with approximately 20dB of gain to bring the microphone signal up to line level. For monaural sampling, the left and right channels of the record mixer can be summed. ODIE also supports monaural recording from either the left or right channel individually.

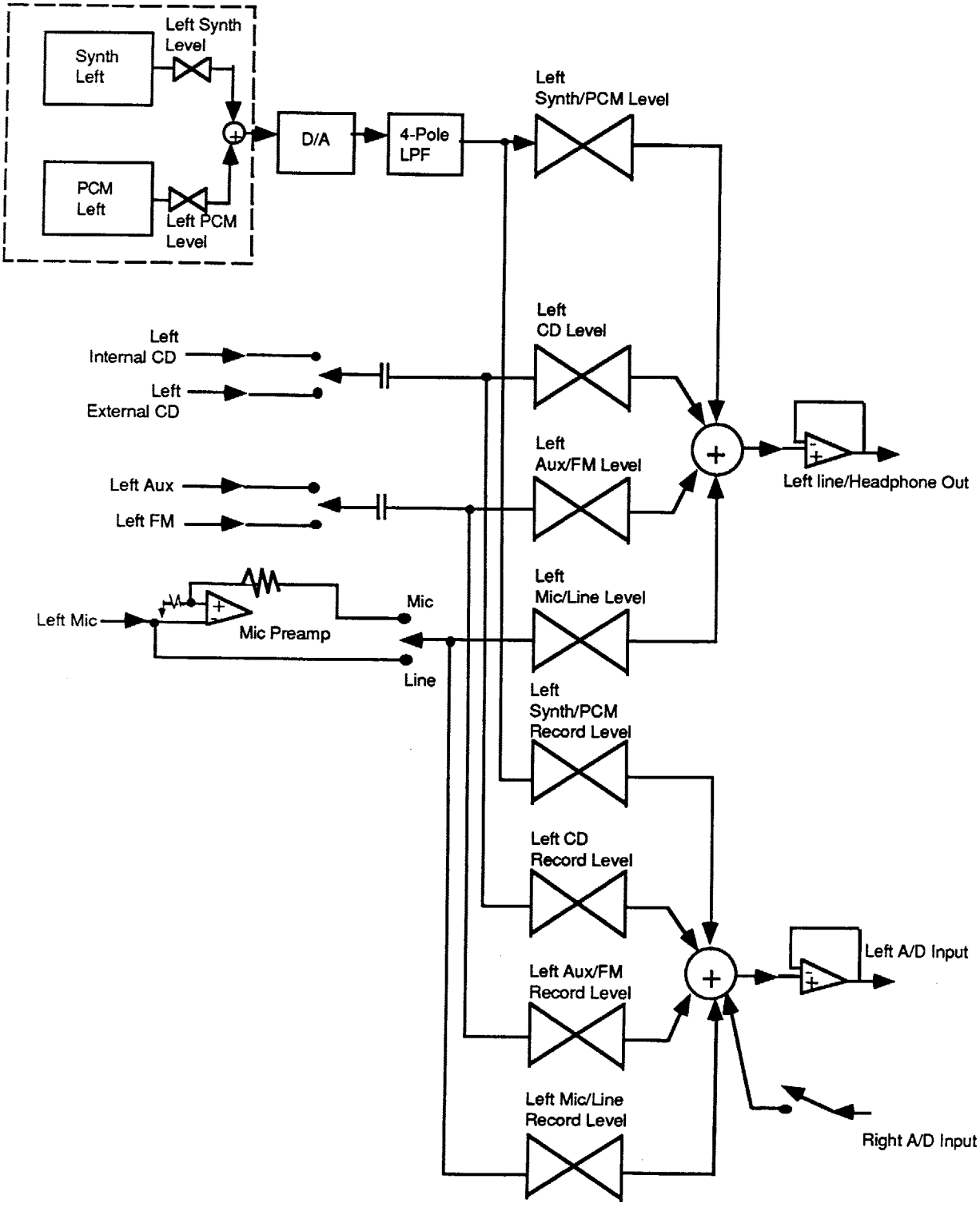


**Figure 3 - Analog Section Block Diagram (Left Channel)**

## SECTION 5 - REGISTER AND PINOUT MAP

### DIRECT-MAPPED HOST I/O REGISTERS:

#### MIDI INTERFACE EMULATION CONTROL/STATUS REGISTER:

ADDRESS: **BASE+0H**

IN MC6850 EMULATION MODE:

ON WRITE:

| | |
|---|---|
| Bits 0-1 | 11b => Reset |
| Bit 2 | 0 => HOST Mode<br>1 => MIDI Mode |
| Bits 3-4 | Ignored |
| Bits 5-6 | 01b => TxRDY Interrupt Enabled |
| Bit 7 | 1 => RxRDY Interrupt Enabled |

ON READ:

| | |
|---|---|
| Bit 0 | 1 => RxRDY, Forced To 0 When Reset |
| Bit 1 | 1 => TxRDY, Forced To 0 When Reset |
| Bit 2 | 0 => MIDI Mode<br>1 => HOST Mode |
| Bits 3-6 | Always 0 |
| Bit 7 | 1 => Interrupt Pending, Forced To 0 When Reset |

IN MPU-401 EMULATION MODE:

READ/WRITE:

| | |
|---|---|
| Bits 0-7 | MPU-401 Emulation Data |

Both the MIDI Emulation and HOST ports may be operated in either MC6850 emulation or MPU-401 emulation modes. The power-up default is MC6850 mode. The operating mode is controlled by the OBP. When in MPU-401 emulation mode, RxRDY interrupts are ALWAYS enabled. For maximum compatibility when operating in MPU-401 emulation mode, the Host Interrupt Configuration register should be programmed to provide a separate interrupt for the MIDI Emulation, otherwise all other interrupts can be blocked by ill-behaved applications software. Because of this, MPU-401 mode may not be generally usable on the HOST interface, but is provided there purely for the sake of symmetry.

#### MIDI INTERFACE EMULATION DATA REGISTER:

ADDRESS: **BASE+1H**

READ/WRITE:

| | |
|---|---|
| Bits 0-7 | MIDI Emulation Data |

IN MPU-401 EMULATION MODE:

ON WRITE:

| | |
|---|---|
| Bits 0-7 | MPU-401 Emulation Command |

ON READ:

| | |
|---|---|
| Bits 0-5 | Always 1 |
| Bit 6 | 0 => TxRDY |
| Bit 7 | 0 => RxRDY |

HOST INTERFACE CONTROL/STATUS REGISTER:

IN MC6850 EMULATION MODE:

ADDRESS: **BASE+2H**

ON WRITE:

| | |
|---|---|
| Bits 0-1 | 11b => Reset |
| Bit 2 | 0 => HOST Mode<br>1 => MIDI Mode |
| Bits 3-4 | Ignored |
| Bits 5-6 | 01b => TxRDY Interrupt Enabled |
| Bit 7 | 1 => RxRDY Interrupt Enabled |

ON READ:

| | |
|---|---|
| Bit 0 | 1 => RxRDY, Forced To 0 When Reset |
| Bit 1 | 1 => TxRDY, Forced To 0 When Reset |
| Bit 2 | 0 => MIDI Mode<br>1 => HOST Mode |
| Bits 3-6 | Always 0 |
| Bit 7 | 1 => Interrupt Pending, Forced To 0 When Reset |

IN MPU-401 EMULATION MODE:

READ/WRITE:

| | |
|---|---|
| Bits 0-7 | MPU-401 Emulation Data |

HOST INTERFACE DATA REGISTER:

ADDRESS: **BASE+3H**

READ/WRITE:

| | |
|---|---|
| Bits 0-7 | HOST Interface Data |

IN MPU-401 EMULATION MODE:

ON WRITE:

| | |
|---|---|
| Bits 0-7 | MPU-401 Emulation Command |

ON READ:

| | |
|---|---|
| Bits 0-5 | Always 1 |
| Bit 6 | 0 => TxRDY |
| Bit 7 | 0 => RxRDY |

ODIE INTERNAL ADDRESS REGISTER:

ADDRESS: **BASE+4H**

READ/WRITE:

| | |
|---|---|
| Bits 0-3 | ODIE Internal Register Address |
| Bits 4-7 | On Write: Ignored<br>On Read: Always 0 |

ODIE INTERNAL DATA REGISTER:

ADDRESS: **BASE+5H**

READ/WRITE:

| | |
|---|---|
| Bits 0-7 | ODIE Internal Register Data |

NOTE - The following regsiters are only present when one of the SoundBlaster emulation modes is enabled in the Host Master Control Register.

SOUNDBLASTER PCM EMULATION RESET REGISTER:

ADDRESS: **226H**

WRITE ONLY:

| | |
|---|---|
| Bit 0 | 0 => Normal Operation<br>1 => Reset SoundBlaster DSP |
| Bits 1-7 | Ignored |

SOUNDBLASTER YM-3812 EMULATION ADDRESS/STATUS REGISTER:

ADDRESS: **228/388H**

ON WRITE:

| | |
|---|---|
| Bits 0-7 | YM-3812 Register Address |

ON READ:

| | |
|---|---|
| Bits 0-7 | Last Data Written To Indirect Register 0CH |

SOUNDBLASTER YM-3812 EMULATION DATA REGISTER:

ADDRESS: 229/389H

WRITE ONLY:

| | |
|---|---|
| Bits 0-7 | YM-3812 Register Data |

When YM-3812 emulation is enabled in the Host Master Control Register, writing to this register will cause an immediate Non-Maskable Interrupt to the Host PC. This interrupt can be cleared either by disabling the emulation, or by writing to the write-only YM-3812 Emulation Status Register (Indirect Register 0CH).

SOUNDBLASTER PCM EMULATION RECEIVED DATA REGISTER:

ADDRESS: 22AH

READ ONLY:

| | |
|---|---|
| Bits 0-7 | SoundBlaster PCM Emulation Received Data |

SOUNDBLASTER PCM EMULATION COMMAND/TXRDY STATUS REGISTER:

ADDRESS: 22CH

ON WRITE:

| | |
|---|---|
| Bits 0-7 | SoundBlaster DSP Command/Data |

ON READ:

| | |
|---|---|
| Bits 0-6 | Always 1 |
| Bit 7 | 0 => TxRDY |

SOUNDBLASTER PCM EMULATION RXRDY STATUS REGISTER:

ADDRESS: 22EH

READ ONLY:

| | |
|---|---|
| Bits 0-6 | Always 1 |
| Bit 7 | 1 => RxRDY |

Reading this register also clears any pending SoundBlaster interrupts.

HOST INTERRUPT STATUS REGISTER (HIS):

ADDRESS: 0H

READ ONLY:

| | |
|---|---|
| Bit 0 | 1 => MIDI Emulation Interrupt Pending |
| Bit 1 | 1 => HOST Interface Interrupt Pending |
| Bits 2-3 | Always 0 |
| Bit 4 | 1 => DMA A Terminal Count Interrupt Pending |
| Bit 5 | 1 => DMA B Terminal Count Interrupt Pending |
| Bit 6 | 1 => MIDI Clock Interrupt Pending |
| Bit 7 | 1 => IRQ Pending |

IRQ Pending (Bit 7) is a logical OR of Bits 0-6. Bits 4-6 are cleared by toggling their respective enables to 0 in the Host Interrupt Enable Register.

ADDRESS: 1H

HOST INTERRUPT ENABLE REGISTER (HIE):

READ/WRITE:

| | |
|---|---|
| Bits 0-3 | On Write: Ignored<br>On Read: Always 0 |
| Bit 4 | 1 => DMA A Terminal Count Interrupt Enabled |
| Bit 5 | 1 => DMA B Terminal Count Interrupt Enabled |
| Bit 6 | 1 => MIDI Clock Interrupt Enabled |
| Bit 7 | 1 => Master Interrupt Enabled |

When operating in Edge-Triggered Interrupt Mode, any write to this register will re-arm the interrupt controller. The DMA and MIDI Clock interrupts are cleared by toggling the respective enable bit to 0.

ADDRESS: 2H

HOST DMA A TRIGGER/STATUS REGISTER (HDAT):

READ/WRITE:

| | |
|---|---|
| Bit 0 | On Write: 1 => DMA A Trigger<br>On Read: 1 => DMA Done |
| Bit 1 | On Write: Ignored<br>On Read: 1 => A/D Overflow |
| Bit 2 | On Write: Ignored<br>On Read: 1 => Code DownLoad Mode Enabled |
| Bit 3 | On Write: Ignored<br>On Read: 1 => Host DRQ Is Asserted |

| | |
|---|---|
| Bits 4-6 | DMA A Host DMA Channel Select<br>000b => Host DMA Channel 0<br>001b => Host DMA Channel 1<br>010b => DMA A Disabled<br>011b => Host DMA Channel 3<br>100b => DMA A Disabled<br>101b => Host DMA Channel 5<br>110b => Host DMA Channel 6<br>111b => Host DMA Channel 7 |
| Bit 7 | Host DMA Channel Size<br>0 => 16-Bit<br>1 => 8-Bit |

DMA transfer on DMA channel A is triggered by writing a 1, then a 0 to bit 0 of this register. The DMA will actually commence on the trailing edge of the second write. Failure to follow this protocol may result in undesired or missed triggers. The DMA channel must first be initialized by the OBP. This is used during startup to trigger the DMA to perform a code download. After reset, both DMA channels are configured for 16-bit Normal In Mode, with a starting address of 000000H. It is important to intialize bit 0 to 0 while the Master Control Register is in RESET mode.

**ADDRESS: 3H**

**HOST DMA B TRIGGER/STATUS REGISTER (HDBT):**

**READ/WRITE:**

| | |
|---|---|
| Bit 0 | On Write: 1 => DMA Trigger<br>On Read: 1 => DMA B Done |
| Bit 1 | On Write: Ignored<br>On Read: 1 => A/D Overflow |
| Bit 2 | On Write: Ignored<br>On Read: 1 => Code DownLoad Mode Enabled |
| Bit 3 | On Write: Ignored<br>On Read: 1 => Host DRQ Is Asserted |
| Bits 4-6 | DMA B Host DMA Channel Select<br>000b => Host DMA Channel 0<br>001b => Host DMA Channel 1<br>010b => DMA B Disabled<br>011b => Host DMA Channel 3<br>100b => DMA B Disabled<br>101b => Host DMA Channel 5<br>110b => Host DMA Channel 6<br>111b => Host DMA Channel 7 |
| Bit 7 | Host DMA Channel Size<br>0 => 16-Bit<br>1 => 8-Bit |

For detailed description of this register, refer to description of DMA A Trigger/Status Register above.

HOST INTERRUPT INTERFACE CONFIGURATION REGISTER (HIC):

ADDRESS: 4H

READ/WRITE:

| | |
|---|---|
| Bits 0-1 | MIDI Emulation IRQ Select<br>00b => IRQ0<br>01b => IRQ1<br>10b => IRQ2<br>11b => IRQ3 |
| Bits 2-3 | Host IRQ Select<br>00b => IRQ0<br>01b => IRQ1<br>10b => IRQ2<br>11b => IRQ3 |
| Bits 4-5 | Host/MIDI Emulation Interrupt Mode Select<br>00b => Edge Sensitive (Sharable)<br>01b => Low Level Sensitive (Sharable)<br>10b => Low Level Sensitive (Non-Sharable)<br>11b => High Level Sensitive (Non-Sharable) |
| Bit 6-7 | CD-ROM Interface Interrupt Mode Select<br>00b => Edge Sensitive (Sharable)<br>01b => Low Level Sensitive (Sharable)<br>10b => Low Level Sensitive (Non-Sharable)<br>11b => High Level Sensitive (Non-Sharable) |

Four different host interrupt interfaces are provided. In Edge Sensitive mode, when an interrupt occurs, a low pulse will be asserted on the selected host IRQ line. The IRQ lines are driven by tri-state drivers which are enabled only when outputting the pulse. In this way, multiple boards may share the same IRQ line. When operating in this mode, it is essential that each interrupt handler perform a write to the Host Interrupt Enable register AFTER issuing an EOI to the host machines interrupt controller. This will cause the interrupt interface to generate another low pulse on the IRQ line if additional interrupts are still pending.

In the Sharable Low Level Sensitive mode, the selected IRQ line is again driven by a tri-state driver, which is enabled only when an interrupt is pending. The selected IRQ line is held low until all pending interrupts are cleared. Since the drivers are enabled only to drive the IRQ line LOW, multiple boards may share the same IRQ line.

The Non-Sharable Low Level Sensitive and Non-Sharable High Level Sensitive modes ALWAYS drive the selected IRQ line, regardless of whether there are pending interrupts. Because of this, only a single board may use a given IRQ line at any one time. This mode, is, however, compatible with the interrupt architecture of most ISA-bus add-in cards, and PC- and

XT-class machines.

### HOST DMA INTERFACE CONFIGURATION REGISTER (HDC):

**ADDRESS:** 5H

**READ/WRITE:**

| | |
|---|---|
| Bits 0-3 | On Write: Ignored<br>On Read: Always 0 |
| Bit 4 | DMA A & B DRQ Polarity<br>0 => Active LOW<br>1 => Active HIGH |
| Bit 5 | DMA A & B DACK Polarity<br>0 => Active LOW<br>1 => Active HIGH |
| Bit 6 | CD-ROM DMA DRQ Polarity<br>0 => INVERTED<br>1 => TRUE |
| Bit 7 | CD-ROM DMA DACK Polarity<br>0 => TRUE<br>1 => INVERTED |

### HOST CD-ROM/SCSI INTERFACE CONFIGURATION REGISTER (HCDC):

**ADDRESS:** 6H

**READ/WRITE:**

| | |
|---|---|
| Bit 0 | CD-ROM Interrupt Enable<br>0 => Disabled<br>1 => Enabled |
| Bits 1-2 | CD-ROM IRQ Select<br>00b => IRQ0<br>01b => IRQ1<br>10b => IRQ2<br>11b => IRQ3 |
| Bit 3 | CD-ROM DMA Enable<br>0 => Disabled<br>1 => Enabled |

| | |
|---|---|
| Bits 4-6 | CD-ROM DMA Channel Select<br>000b => Host DMA Channel 0<br>001b => Host DMA Channel 1<br>010b => CD-ROM DMA Disabled<br>011b => Host DMA Channel 3<br>100b => CD-ROM DMA Disabled<br>101b => Host DMA Channel 5<br>110b => Host DMA Channel 6<br>111b => Host DMA Channel 7 |
| Bit 7 | CD-ROM Interface Enable<br>0 => Disabled<br>1 => Enabled |

Note that to minimize interaction between the S-1000 and the CD-ROM, this register is not affected by subsystem resets. Only a hardware (power-up) reset will clear this register.

SOUND MEMORY CONFIGURATION REGISTER A (HMCA):

ADDRESS: 7H

READ/WRITE:

| | |
|---|---|
| Bit 0 | Device 0 Memory Type<br>0 => DRAM<br>1 => ROM/SRAM |
| Bit 1 | Device 1 Memory Type<br>0 => DRAM<br>1 => ROM/SRAM |
| Bit 2 | Device 2 Memory Type<br>0 => DRAM<br>1 => ROM/SRAM |
| Bit 3 | Device 3 Memory Type<br>0 => DRAM<br>1 => ROM/SRAM |
| Bits 4-6 | Sound Memory Device Size Select<br>000b => 8Mw<br>001b => 4Mw<br>010b => 2Mw<br>011b => 1Mw<br>100b => 512Kw<br>101b => 256Kw<br>110b => 128Kw<br>111b => 64Kw |
| Bit 7 | CAS4 Function Select<br>0 => CAS4 = CAS1+CAS2<br>1 => CAS4 = CAS0+CAS1 |

SOUND MEMORY CONFIGURATION REGISTER B (HMCB):

ADDRESS: 8H

READ/WRITE:

| | |
|---|---|
| Bits 0-1 | DRAM 0 Size<br>00b => 64K<br>01b => 256K<br>10b => 1M<br>11b => 4M |
| Bits 2-3 | DRAM 1 Size<br>00b => 64K<br>01b => 256K<br>10b => 1M<br>11b => 4M |
| Bits 4-5 | DRAM 2 Size<br>00b => 64K<br>01b => 256K<br>10b => 1M<br>11b => 4M |
| Bits 6-7 | DRAM 3 Size<br>00b => 64K<br>01b => 256K<br>10b => 1M<br>11b => 4M |

HOST MASTER CONTROL REGISTER (HMC):

ADDRESS: 9H

READ/WRITE:

| | |
|---|---|
| Bits 0-1 | SoundBlaster Emulation Mode Select:<br>00b => SoundBlaster Emulation Disabled<br>01b => SoundBlaster + OPL-2 Enabled<br>10b => SoundBlaster + OPL-3 Enabled<br>11b => SoundBlaster + OPL-2 Emulation Enabled |
| Bit 2 | AdLib Yamaha FM Address:<br>0 => OPL-2/Emulation Disabled At 388-389H<br>1 => OPL-2/Emulation Enabled At 388-389H |
| Bit 3 | 0 => Joystick Interface Disabled<br>1 => JoyStick Interface Enabled |
| Bits 4-5 | 00b => CD-ROM At Base + 6 thru Base + 7<br>01b => CD-ROM At Base + 8 thru Base + 15<br>10b => CD-ROM At Base + 16 thru Base + 31<br>11b => CD-ROM At Base + 16 thru Base + 47 |

| | |
|---|---|
| Bits 6-7 | Subsystem Master Control Bits<br>00b => Subsystem Hardware Reset<br>01b => Normal Operation<br>OBP Enabled, DMA Disabled, Refresh Disabled<br>10b => Code Download Mode<br>OBP Suspended, DMA Enabled, Refresh Enabled<br>11b => OBP Startup Mode<br>OBP Enabled, DMA Disabled, Refresh Enabled |

**YM-3812 EMULATION ADDRESS REGISTER (HFMA):**

**ADDRESS:** **AH**

**READ ONLY:**

| | |
|---|---|
| Bits 0-7 | Last Data Written To Host Port 228H |

**YM-3812 EMULATION DATA REGISTER (HFMD):**

**ADDRESS:** **BH**

**READ ONLY:**

| | |
|---|---|
| Bits 0-7 | Last Data Written To Host Port 229H |

**YM-3812 EMULATION STATUS REGISTER (HFMS):**

**ADDRESS:** **CH**

**WRITE ONLY:**

| | |
|---|---|
| Bits 0-7 | YM-3812 Emulation Status |

Any write to this register will clear a pending NMI.

**DIRECT-MAPPED ON-BOARD PROCESSOR REGISTERS:** **MIDI INTERFACE EMULATION CONTROL/STATUS REGISTER:**

**ADDRESS:** **A00000H**

**READ/WRITE:**

| | |
|---|---|
| Bit 0 | On Write: Ignored<br>On Read: 1 => RxRDY, Forced To 0 When Reset |
| Bit 1 | On Write: Ignored<br>On Read: 1 => TxRDY, Forced To 0 When Reset |
| Bit 2 | 0 => Data Register Contains MIDI/Data Byte<br>1 => Data Register Contains HOST/Command Byte |
| Bit 3 | 0 => MIDI Mode<br>1 => HOST Mode |

| | |
|---|---|
| Bit 4 | 0 => MC6850 Mode<br>1 => MPU-401 Mode |
| Bit 5 | On Write: Ignored<br>On Read: HOST Reset Status:<br>0 => Reset<br>1 => Normal Operation |
| Bit 6 | 1 => TxRDY Interrupt Enabled |
| Bit 7 | 1 => RxRDY Interrupt Enabled |

The interface is reset by writing 11b to bits 3 and 4.

MIDI INTERFACE EMULATION DATA REGISTER:

ADDRESS: **A00001H**

READ/WRITE:

| | |
|---|---|
| Bits 0-7 | MIDI Emulation Data |

HOST INTERFACE CONTROL/STATUS REGISTER:

ADDRESS: **A00002H**

READ/WRITE:

| | |
|---|---|
| Bit 0 | On Write: Ignored<br>On Read: 1 => RxRDY, Forced To 0 When Reset |
| Bit 1 | On Write: Ignored<br>On Read: 1 => TxRDY, Forced To 0 When Reset |
| Bit 2 | 0 => Data Register Contains MIDI/Data Byte<br>1 => Data Register Contains HOST/Command Byte |
| Bit 3 | 0 => MIDI Mode<br>1 => HOST Mode |
| Bit 4 | 0 => MC6850 Mode<br>1 => MPU-401 Mode |
| Bit 5 | HOST Reset Status:<br>0 => Reset<br>1 => Normal Operation |
| Bit 6 | 1 => TxRDY Interrupt Enabled |
| Bit 7 | 1 => RxRDY Interrupt Enabled |

The interface is reset by writing 11b to bits 3 and 4.

HOST INTERFACE DATA REGISTER:

ADDRESS: A00003H

READ/WRITE:

| | |
|---|---|
| Bits 0-7 | HOST Interface Data |

MIDI INTERFACE CONTROL/STATUS REGISTER:

ADDRESS: A00004H

READ/WRITE:

| | |
|---|---|
| Bit 0 | 1 => RxRDY |
| Bit 1 | 1 => TxRDY |
| Bit 2 | On Write: Ignored<br>On Read: Always 0 |
| Bits 3-4 | 11b => Reset |
| Bit 5 | On Write: Ignored<br>On Read: Reset Status<br>0 => Reset<br>1 => Normal Operation |
| Bit 6 | 1 => TxRDY Interrupt Enabled |
| Bit 7 | 1 => RxRDY Interrupt Enabled |

MIDI INTERFACE DATA REGISTER:

ADDRESS: A00005H

READ/WRITE:

| | |
|---|---|
| Bits 0-7 | MIDI Data |

INTERRUPT CONTROL REGISTER:

ADDRESS: A00006H

READ/WRITE:

| | |
|---|---|
| Bits 0-2 | On Write: Ignored<br>On Read: Always 0 |
| Bit 3 | 1 => OTTO Interrupt Enabled |
| Bit 4 | 1 => Timer Interrupt Enabled |
| Bit 5 | 1 => DMA A Terminal Count Interrupt Enabled |
| Bit 6 | 1 => DMA B Terminal Count Interrupt Enabled |
| Bit 7 | 1 => MIDI Clock Interrupt Enabled |

INTERRUPT STATUS/YM-3812 STATUS REGISTER:

ADDRESS: A00007H

ON READ:

| | |
|---|---|
| Bit 0 | 1 => MIDI Interface Interrupt Pending |
| Bit 1 | 1 => OTTO Interrupt Pending |
| Bit 2 | 1 => Host Interface Interrupt Pending |
| Bit 3 | 1 => MIDI Emulation Interface Interrupt Pending |
| Bit 4 | 1 => Timer Interrupt Pending |
| Bit 5 | 1 => DMA A Complete Interrupt Pending |
| Bit 6 | 1 => DMA B Complete Interrupt Pending |
| Bit 7 | 1 => MIDI Clock/SoundBlaster Interrupt Pending |

ON WRITE:

| | |
|---|---|
| Bits 0-7 | YM-3812 Emulation Status |

On read, this register gives the current status of all interrupt sources. The Timer, DMA, and MIDI Clock interrupts are cleared by toggling their respective enable bits LOW. The SoundBlaster interrupt is cleared by writing the SoundBlaster control register. The DMA complete interrupts will occur on one of two conditions depending on DMA mode. For normal (sample data) transfers these interrupts will occur on Terminal Count. For PCM and A/D transfers, these interrupts will occur at the end of each buffer transfer (2K samples). On write, data is written to the Host YM-3812 Emulation Status Register. Note that there is NO arbitration, so this register must not be simultaneously written by the OBP and the HOST, or results will be unpredictable.

DMA A CONTROL REGISTER:

ADDRESS: A00008H

READ/WRITE:

| | |
|---|---|
| Bits 0-1 | DMA Mode<br>00b => Disabled (Reset)<br>01b => Normal Mode<br>10b => PCM Playback Mode<br>11b => A/D Record Mode |
| Bit 2 | In Modes 0-2: DMA Direction<br>0 => DMA In (From Host)<br>1 => DMA Out (To Host)<br>In Mode 3: A/D Data Format<br>0 => I2S Format (Left Justified)<br>1 => Japanese Format (Right Justified) |

| | |
|---|---|
| Bit 3 | Data Type<br>0 => Non-Interleaved/Mono<br>1 => Interleaved Stereo |
| Bits 4-5 | Data Size<br>00b => 16-Bit Linear<br>01b => 12-Bit Linear<br>10b => 8-Bit Linear<br>11b => μ-Law Compressed |
| Bit 6 | Data Format<br>0 => Signed<br>1 => Unsigned |
| Bit 7 | DMA Halt<br>0 => DMA Transfer Enabled<br>1 => DMA Transfer Halted |

The DMA Mode bits, when both 0, places the DMA hardware in a RESET state, immediately stopping any transfer in process. To perform a DMA transfer, the DMA Control Register should first be initialized, then perform a write to the DMA Trigger register to begin the transfer of data. To terminate a transfer before reaching Terminal Count (or other normal termination criteria), the DMA Control register should be written again with the DMA Halt bit SET. Any single sample transfer currently in progress will be completed, and then the DMA hardware will return to an idle state. Note that when a transfer is stopped using the HALT bit, the transfer will actually halt after the next sample, if MONO mode, or after the next pair of samples if STEREO mode. After being HALTed, a transfer can be restarted from where it left off by again writing to the DMA Trigger register, or the DMA Address Registers can be read to determine the exact number of samples remaining in the buffer. Note that in the case of A/D transfers, both DMA channels are used. One will be set to A/D mode, to read data from the A/D converter into memory, the other will be set to PCM mode, to transfer the data from memory to the host. In this mode, the trigger for the PCM channel is provided automatically by the A/D channel, so it is important that the A/D channel be stopped first, to prevent the PCM channel from being re-triggered after it is stopped. Issuing a trigger to a DMA channel that is not stopped may result in anomolous behavior.

**DMA A TRIGGER/STATUS REGISTER:**

**ADDRESS:** **A00009H**

**ON WRITE:**

| | |
|---|---|
| Bits 0-7 | Ignored: Any Write Triggers DMA |

**ON READ:**

| | |
|---|---|
| Bit 0 | 1 => DMA Done |
| Bit 1 | 1 => A/D Overflow |
| Bit 2 | 1 => Code Download Mode Enabled |
| Bit 3 | 1 => Host DMA Channel Is 8-Bit |
| Bit 4 | 1 => Host DRQ Is Asserted |

| | |
|---|---|
| Bit 5 | 1 => Memory Request Is Asserted |
| Bit 6 | 1 => Left Channel A/D Request Is Asserted |
| Bit 7 | 1 => Right Channel A/D Request Is Asserted |

DMA A ADDRESS REGISTERS:

ADDRESS: A0000A-BH WORD ADDRESSABLE ONLY

READ/WRITE:

| | |
|---|---|
| Bits 0-6 | DMA A Buffer Address Bits 16-22 |
| Bit 7 | On Write: Ignored<br>On Read: Always 0 |
| Bits 8-15 | On Write: Ignored<br>On Read: Current YM3812 Emulation Address |

ADDRESS: A0000C-DH WORD ADDRESSABLE ONLY

READ/WRITE:

| | |
|---|---|
| Bits 0-15 | DMA A Buffer Address Bits 0-15 |

DMA B CONTROL REGISTER:

ADDRESS: A0000EH

READ/WRITE:

| | |
|---|---|
| Bits 0-1 | DMA Mode<br>00b => Disabled (Reset)<br>01b => Normal Mode<br>10b => PCM Playback Mode<br>11b => A/D Record Mode |
| Bit 2 | In Modes 0-2: DMA Direction<br>0 => DMA In (From Host)<br>1 => DMA Out (To Host)<br>In Mode 3: A/D Data Format<br>0 => I2S Format (Left Justified)<br>1 => Japanese Format (Right Justified) |
| Bit 3 | Data Type<br>0 => Non-Interleaved/Mono<br>1 => Interleaved Stereo |
| Bits 4-5 | Data Size<br>00b => 16-Bit Linear<br>01b => 12-Bit Linear<br>10b => 8-Bit Linear<br>11b => μ-Law Compressed |

| | |
|---|---|
| Bit 6 | Data Format<br>0 => Signed<br>1 => Unsigned |
| Bit 7 | DMA Halt<br>0 => DMA Transfer Enabled<br>1 => DMA Transfer Halted |

For operational details, see the DMA A Control register description above.

### DMA B Trigger/Status Register:

**Address:** **A0000Fh**

**On Write:**

| | |
|---|---|
| Bits 0-7 | Ignored: Any Write Triggers DMA |

**On Read:**

| | |
|---|---|
| Bit 0 | 1 => DMA Done |
| Bit 1 | 1 => A/D Overflow |
| Bit 2 | Unused, Always 0 |
| Bit 3 | 1 => Host DMA Channel Is 8-Bit |
| Bit 4 | 1 => Host DMA Request Is Asserted |
| Bit 5 | 1 => Memory Request Is Asserted |
| Bit 6 | 1 => Left Channel A/D Request Is Asserted |
| Bit 7 | 1 => Right Channel A/D Request Is Asserted |

### DMA B Address Registers:

**Address:** **A00010-11h** **Word Addressable Only**

**Read/Write:**

| | |
|---|---|
| Bits 0-6 | DMA B Buffer Address Bits 16-22 |
| Bit 7 | On Write: Ignored<br>On Read: Always 0 |
| Bits 8-15 | On Write: Ignored<br>On Read: Current YM3812 Emulation Data |

**Address:** **A00012-13h** **Word Addressable Only**

**Read/Write:**

| | |
|---|---|
| Bits 0-15 | DMA B Buffer Address Bits 0-15 |

MIDI CLOCK COUNT REGISTER:

ADDRESS: A00014-15H WORD ADDRESSABLE ONLY

READ/WRITE:

| | |
|---|---|
| Bits 0-11 | MIDI Clock Count Bits 0-11 |
| Bits 12-15 | On Write: Ignored<br>On Read: Always 0 |

PWM COUNT REGISTERS:

ADDRESS: A00016H

READ/WRITE:

| | |
|---|---|
| Bit 0 | 0 => Digital Out Mode<br>1 => PWM Mode |
| Bits 1-7 | PWM0 Duty Cycle |

When Bit 0 is 0, Bit 1 is connected directly to the PWMA pin. When Bit 0 is 1, the PWM0 output is connected to the PWMA pin.

ADDRESS: A00017H

READ/WRITE:

| | |
|---|---|
| Bit 0 | 0 => Digital Out Mode<br>1 => PWM Mode |
| Bits 1-7 | PWM1 Duty Cycle |

When Bit 0 is 0, Bit 1 is connected directly to the PWMB pin. When Bit 0 is 1, the PWM1 output is connected to the PWMB pin.

ADDRESS: A00018H

READ/WRITE:

| | |
|---|---|
| Bit 0 | 0 => Digital Out Mode<br>1 => PWM Mode |
| Bits 1-7 | PWM2 Duty Cycle |

When Bit 0 is 0, Bit 6 of the OBP A/D Control Register is connected directly to the PWMC pin. When Bit 0 is 1, the PWM2 output is connected to the PWMC pin.

ADDRESS: A00019H

READ/WRITE:

| | |
|---|---|
| Bit 0 | 0 => Digital Out Mode<br>1 => PWM Mode |

| | |
|---|---|
| Bits 1-7 | PWM3 Duty Cycle |

When Bit 0 is 0, Bit 7 of the OBP A/D Control Register is connected directly to the PWMD pin. When Bit 0 is 1, the PWM3 output is connected to the PWMD pin.

A/D CONTROL REGISTER:

ADDRESS: **A0001AH**

READ/WRITE:

| | |
|---|---|
| Bits 0-7 | A/D Control Bits (ADCTL0-7) |

Bits 0-5 are output on the dedicated ACTL0-5 pins, while bits 6 & 7 are output on the PWMC & PWMD output pins. See the descriptions of the PWM count registers for details of how these outputs are configured and controlled.

MISCELLANEOUS CONTROL REGISTER:

ADDRESS: **A0001BH**

READ/WRITE:

| | |
|---|---|
| Bits 0-1 | OBP Sound Memory Bank Select<br>00b => Bank 0<br>00b => Bank 1<br>10b => Bank 2<br>11b => Bank 3 |
| Bits 2-3 | OBP F-Page Memory CAS/CS Select<br>00b => CAS0*/CS0*<br>00b => CAS1*/CS1*<br>10b => CAS2*/CS2*<br>11b => CAS3*/CS3* |
| Bits 4-5 | Timer Interrupt Rate Select<br>00b => 1 mSec<br>01b => 2 mSec<br>10b => 4 mSec<br>11b => 8 mSec |
| Bit 6 | 1 => OTTO PCM Playback Mode Enabled |
| Bit 7 | 1 => Code Download/Auto Refresh Mode Disabled |

OBP MISCELLANEOUS STATUS REGISTER:

ADDRESS: **A0001CH**

READ ONLY:

| | |
|---|---|
| Bit 0 | Device 0 Memory Type<br>0 => DRAM<br>1 => ROM/SRAM |

| | |
|---|---|
| Bit 1 | Device 1 Memory Type<br>0 => DRAM<br>1 => ROM/SRAM |
| Bit 2 | Device 2 Memory Type<br>0 => DRAM<br>1 => ROM/SRAM |
| Bit 3 | Device 3 Memory Type<br>0 => DRAM<br>1 => ROM/SRAM |
| Bits 4-6 | Sound Memory Device Size Select<br>000b => 8Mw<br>001b => 4Mw<br>010b => 2Mw<br>011b => 1Mw<br>100b => 512Kw<br>101b => 256Kw<br>110b => 128Kw<br>111b => 64Kw |
| Bit 7 | Always 0 |

**TEST MODE CONTROL/STATUS REGISTER:**

**ADDRESS:** **A0001DH**

**READ/WRITE:**

| | |
|---|---|
| Bit 0 | 1 => UART Loopback Mode Enabled |
| Bit 1 | 1 => DMA Address Counter Test Mode Enabled |
| Bit 2 | 1 => A/D Interface Test Mode Enabled |
| Bit 3 | 1 => Timer Turbo Mode Enabled |
| Bit 4 | 1 => Edge-Triggered Interrupt Test Mode Enabled |
| Bit 5 | 1 => DMA A A/D Interface Test Output Enabled |
| Bit 6 | 1 => DMA B A/D Interface Test Output Enabled |
| Bit 7 | 1 => A/D DMA Trigger Disabled |

**SOUNDBLASTER PCM CONTROL/STATUS REGISTER:**

**ADDRESS:** **A0001EH**

**READ/WRITE:**

| | |
|---|---|
| Bit 0 | 1 => RxRDY |
| Bit 1 | 1 => TxRDY |
| Bit 2 | On Write: Ignored<br>On Read: HOST Reset Register Writtten Flag<br>1 => Reset Register Written |
| Bit 3 | 0 => HOST Interface Is Polled<br>1 => HOST Interface Is Interrupt-Driven |

| | |
|---|---|
| Bit 4 | On Write: 0->1 Transition Generates Interrupt To Host<br>On Read: Always 0 |
| Bit 5 | On Write: Ignored<br>On Read: HOST Reset Status<br>0 => Normal Operation<br>1 => Reset |
| Bit 6 | 1 => TxRDY Interrupt Enabled |
| Bit 7 | 1 => RxRDY Interrupt Enabled |

The OBP will be interrupted any time the HOST SoundBlaster PCM Emulation Reset Register is written. Bit 2 of this register will be set to indicate that a HOST Reset was the source of a pending interrupt. Bit 2 will remain set until this register is again written. Bit 5 indicates the current state of the HOST Reset bit. HOST Reset interrupts are cleared by clearing the RxRDY Interrupt Enable (Bit 7). RxRDY/TxRDY interrupts are automatically cleared by reading/writing the SoundBlaster PCM Data Register.

**SOUNDBLASTER PCM DATA REGISTER:**

**ADDRESS:** **A0001FH**

**READ/WRITE:**

| | |
|---|---|
| Bits 0-7 | SoundBlaster Emulation Command/Data |

**PIN ASSIGNMENTS:**

| PIN# | EXT. NAME | INT. NAME | TYPE | DESCRIPTION |
|---|---|---|---|---|
| 1 | GND | | PWR | |
| 2 | GND | | PWR | |
| 3 | HD0 | DH0 | I/O | Host PC Data Bit 0 |
| 4 | HD1 | DH1 | I/O | Host PC Data Bit 1 |
| 5 | HD2 | DH2 | I/O | Host PC Data Bit 2 |
| 6 | HD3 | DH3 | I/O | Host PC Data Bit 3 |
| 7 | HD4 | DH4 | I/O | Host PC Data Bit 4 |
| 8 | HD5 | DH5 | I/O | Host PC Data Bit 5 |
| 9 | HD6 | DH6 | I/O | Host PC Data Bit 6 |
| 10 | HRST | MRST | IN | |
| 11 | HD7 | DH7 | I/O | Host PC Data Bit 7 |
| 12 | HDLE* | DLEH | OUT | Host PC Data Bus Lower Byte Enable |
| 13 | BASE0 | BAS0 | IN | Base Address Select 0 |
| 14 | BASE1 | BAS1 | IN | Base Address Select 1 |

| | | | | |
|---|---|---|---|---|
| 15 | YCS*/NMI | CSYM | OUT | Yamaha Chip Select/NMI |
| 16 | JSRD* | RDJS | OUT | Joystick Read |
| 17 | JSWR* | WRJS | OUT | Joystick Write |
| 18 | PWM0 | PWM0 | OUT | Pulse Width Modulator 0 |
| 19 | PWM1 | PWM1 | OUT | Pulse Width Modulator 1 |
| 20 | PWM2 | PWM2 | OUT | Pulse Width Modulator 2 |
| 21 | PWM3 | PWM3 | OUT | Pulse Width Modulator 3 |
| 22 | ACTL0 | AC0 | OUT | Analog Control Bit 0 |
| 23 | ACTL1 | AC1 | OUT | Analog Control Bit 1 |
| 24 | ACTL2 | AC2 | OUT | Analog Control Bit 2 |
| 25 | ACTL3 | AC3 | OUT | Analog Control Bit 3 |
| 26 | GND | | PWR | |
| 27 | VCC | | PWR | |
| 28 | ACTL4 | AC4 | OUT | Analog Control Bit 4 |
| 29 | ACTL5 | AC5 | OUT | Analog Control Bit 5 |
| 30 | ADDATA | ADD | I/O | A/D Converter Serial Data |
| 31 | ADBCLK | ABC | I/O | A/D Converter Bit Clock |
| 32 | ADLRCLK | ALR | I/O | A/D Converter L/R Clock |
| 33 | RXD | MRXD | IN | MIDI Receive Data |
| 34 | TXD | MTXD | OUT | MIDI Transmit Data |
| 35 | OSCI | OSCI | IN | 32 MHz Oscillator Buffer In |
| 36 | OSCO | OSCO | OUT | 32 MHz Oscillator Buffer Out |
| 37 | PCLK | CLKP | OUT | Processor Clock |
| 38 | DTACK* | ACKP | O/D | Processor Data Transfer Acknowledge |
| 39 | PRW | RWP | IN | Processor R/W |
| 40 | PLDS* | LDSP | IN | Processor Lower Data Strobe |
| 41 | PUDS* | UDSP | IN | Processor Upper Data Strobe |
| 42 | PAS* | ASP | IN | Processor Address Strobe |
| 43 | PD0 | DP0 | I/O | Processor Data Bit 0 |
| 44 | PD1 | DP1 | I/O | Processor Data Bit 1 |
| 45 | PD2 | DP2 | I/O | Processor Data Bit 2 |
| 46 | PD3 | DP3 | I/O | Processor Data Bit 3 |
| 47 | PD4 | DP4 | I/O | Processor Data Bit 4 |
| 48 | PD5 | DP5 | I/O | Processor Data Bit 5 |
| 49 | PD6 | DP6 | I/O | Processor Data Bit 6 |
| 50 | PD7 | DP7 | I/O | Processor Data Bit 7 |
| 51 | GND | | PWR | |
| 52 | GND | | PWR | |
| 53 | VCC | | PWR | |
| 54 | NC | | — | |
| 55 | PD8 | DP8 | I/O | Processor Data Bit 8 |
| 56 | PD9 | DP9 | I/O | Processor Data Bit 9 |
| 57 | PD10 | DPA | I/O | Processor Data Bit 10 |
| 58 | PD11 | DPB | I/O | Processor Data Bit 11 |

| | | | | |
|---|---|---|---|---|
| 59 | PD12 | DPC | I/O | Processor Data Bit 12 |
| 60 | PD13 | DPD | I/O | Processor Data Bit 13 |
| 61 | PD14 | DPE | I/O | Processor Data Bit 14 |
| 62 | PD15 | DPF | I/O | Processor Data Bit 15 |
| 63 | PA23 | APN | IN | Processor Address Bit 23 |
| 64 | PA22 | APM | IN | Processor Address Bit 22 |
| 65 | PA21 | APL | IN | Processor Address Bit 21 |
| 66 | PA20 | APK | IN | Processor Address Bit 20 |
| 67 | PA19 | APJ | IN | Processor Address Bit 19 |
| 68 | PA18 | API | IN | Processor Address Bit 18 |
| 69 | PA17 | APH | IN | Processor Address Bit 17 |
| 70 | PA16 | APG | IN | Processor Address Bit 16 |
| 71 | PA15 | APF | IN | Processor Address Bit 15 |
| 72 | PA14 | APE | IN | Processor Address Bit 14 |
| 73 | PA13 | APD | IN | Processor Address Bit 13 |
| 74 | PA12 | APC | IN | Processor Address Bit 12 |
| 75 | PA11 | APB | IN | Processor Address Bit 11 |
| 76 | PA10 | APA | IN | Processor Address Bit 10 |
| 77 | PA9 | AP9 | IN | Processor Address Bit 9 |
| 78 | VCC | | PWR | |
| 79 | GND | | PWR | |
| 80 | PA8 | AP8 | IN | Processor Address Bit 8 |
| 81 | PA7 | AP7 | IN | Processor Address Bit 7 |
| 82 | PA6 | AP6 | IN | Processor Address Bit 6 |
| 83 | PA5 | AP5 | IN | Processor Address Bit 5 |
| 84 | PA4 | AP4 | IN | Processor Address Bit 4 |
| 85 | PA3 | AP3 | IN | Processor Address Bit 3 |
| 86 | PA2 | AP2 | IN | Processor Address Bit 2 |
| 87 | PA1 | AP1 | IN | Processor Address Bit 1 |
| 88 | FC0 | FC0P | IN | Processor Function Code 0 |
| 89 | FC1 | FC1P | IN | Processor Function Code 1 |
| 90 | IPL0* | IPL0 | OUT | Processor Interrupt Priority 0 |
| 91 | IPL1* | IPL1 | OUT | Processor Interrupt Priority 1 |
| 92 | IPL2* | IPL2 | OUT | Processor Interrupt Priority 2 |
| 93 | PRST* | RSTP | O/D | Processor Reset |
| 94 | PHLT* | HLTP | O/D | Processor Halt |
| 95 | DABCLK | DBC | I/O | D/A Converter Bit Clock |
| 96 | DALRCLK | DLR | I/O | D/A Converter L/R Clock |
| 97 | DADATA | DAD | I/O | D/A Converter Serial Data |
| 98 | AD15 | AOK | I/O | Sound Memory Address/Data Bit 15 |
| 99 | AD14 | AOJ | I/O | Sound Memory Address/Data Bit 14 |
| 100 | AD13 | AOI | I/O | Sound Memory Address/Data Bit 13 |
| 101 | AD12 | AOH | I/O | Sound Memory Address/Data Bit 12 |
| 102 | AD11 | AOG | I/O | Sound Memory Address/Data Bit 11 |

| | | | | |
|---|---|---|---|---|
| 103 | NC | | — | |
| 104 | VCC | | PWR | |
| 105 | GND | | PWR | |
| 106 | GND | | PWR | |
| 107 | AD10 | AOF | I/O | Sound Memory Address/Data Bit 10 |
| 108 | AD9 | AOE | I/O | Sound Memory Address/Data Bit 9 |
| 109 | AD8 | AOD | I/O | Sound Memory Address/Data Bit 8 |
| 110 | AD7 | AOC | I/O | Sound Memory Address/Data Bit 7 |
| 111 | AD6 | AOB | I/O | Sound Memory Address/Data Bit 6 |
| 112 | AD5 | AOA | I/O | Sound Memory Address/Data Bit 5 |
| 113 | AD4 | AO9 | I/O | Sound Memory Address/Data Bit 4 |
| 114 | AD3 | AO8 | I/O | Sound Memory Address/Data Bit 3 |
| 115 | AD2 | AO7 | I/O | Sound Memory Address/Data Bit 2 |
| 116 | AD1 | AO6 | I/O | Sound Memory Address/Data Bit 1 |
| 117 | AD0 | AO5 | I/O | Sound Memory Address/Data Bit 0 |
| 118 | OA4 | AO4 | I/O | Sound Memory Address Bit 4 |
| 119 | OA3 | AO3 | I/O | Sound Memory Address Bit 3 |
| 120 | OA2 | AO2 | I/O | Sound Memory Address Bit 2 |
| 121 | OA1 | AO1 | I/O | Sound Memory Address Bit 1 |
| 122 | OA0 | AO0 | I/O | Sound Memory Address Bit 0 |
| 123 | OA22 | AOM | I/O | Sound Memory Address Bit 22 |
| 124 | OA21 | AOL | I/O | Sound Memory Address Bit 21 |
| 125 | OIRQ* | IRQO | IN | OTTO Interrupt Request |
| 126 | OCLK | CLKO | OUT | OTTO 16 MHz Master Clock |
| 127 | ECLK | CLKE | OUT | OTTO E Clock |
| 128 | OCS* | CSO | OUT | OTTO Chip Select |
| 129 | AMUX | AMUX | OUT | Address MUX Control |
| 130 | VCC | | PWR | |
| 131 | GND | | PWR | |
| 132 | UWEN* | UWEN | OUT | Sound Memory Upper Byte Write Enable |
| 133 | LWEN* | LWEN | OUT | Sound Memory Lower Byte Write Enable |
| 134 | RAS* | RAS | OUT | Sound Memory Row Address Strobe |
| 135 | CAS0* | CAS0 | OUT | Sound Memory Column Address Strobe 0 |
| 136 | CAS1* | CAS1 | OUT | Sound Memory Column Address Strobe 1 |
| 137 | CAS2* | CAS2 | OUT | Sound Memory Column Address Strobe 2 |
| 138 | CAS3* | CAS3 | OUT | Sound Memory Column Address Strobe 3 |
| 139 | CAS4* | CAS4 | OUT | Sound Memory Column Address Strobe 4 |
| 140 | XA0 | XA0 | OUT | Multiplexed Sound Memory Address Bit 0 |
| 141 | XA1 | XA1 | OUT | Multiplexed Sound Memory Address Bit 1 |
| 142 | XA2 | XA2 | OUT | Multiplexed Sound Memory Address Bit 2 |
| 143 | XA3 | XA3 | OUT | Multiplexed Sound Memory Address Bit 3 |
| 144 | XA4 | XA4 | OUT | Multiplexed Sound Memory Address Bit 4 |
| 145 | XA5 | XA5 | OUT | Multiplexed Sound Memory Address Bit 5 |
| 146 | XA6 | XA6 | OUT | Multiplexed Sound Memory Address Bit 6 |

| | | | | |
|---|---|---|---|---|
| 147 | XA7 | XA7 | OUT | Multiplexed Sound Memory Address Bit 7 |
| 148 | XA8 | XA8 | OUT | Multiplexed Sound Memory Address Bit 8 |
| 149 | XA9 | XA9 | OUT | Multiplexed Sound Memory Address Bit 9 |
| 150 | XA10 | XA10 | OUT | Multiplexed Sound Memory Address Bit 10 |
| 151 | LA5 | LA5 | OUT | Latched Sound Memory Address Bit 5 |
| 152 | LA6 | LA6 | OUT | Latched Sound Memory Address Bit 6 |
| 153 | LA7 | LA7 | OUT | Latched Sound Memory Address Bit 7 |
| 154 | LA8 | LA8 | OUT | Latched Sound Memory Address Bit 8 |
| 155 | GND | | PWR | |
| 156 | GND | | PWR | |
| 157 | VCC | | PWR | |
| 158 | NC | | — | |
| 159 | LA9 | LA9 | OUT | Latched Sound Memory Address Bit 9 |
| 160 | CDCS* | CSCD | OUT | CD-ROM Interface Chip Select |
| 161 | CDIRQ | IRCD | IN | CD-ROM Interface Interrupt Request |
| 162 | CDDRQ | DRCD | IN | CD-ROM Interface DMA Request |
| 163 | CDDACK | ACD | OUT | CD-ROM Interface DMA Acknowledge |
| 164 | CDRST* | RSTC | OUT | CD-ROM Interface Reset |
| 165 | HD15 | DHF | I/O | Host PC Data Bit 15 |
| 166 | HD14 | DHE | I/O | Host PC Data Bit 14 |
| 167 | HD13 | DHD | I/O | Host PC Data Bit 13 |
| 168 | HDRQ7 | RQ7 | OUT | Host PC Channel 7 DMA Request |
| 169 | HD12 | DHC | I/O | Host PC Data Bit 12 |
| 170 | HDACK7 | ACK7 | IN | Host PC Channel 7 DMA Acknowledge |
| 171 | HD11 | DHB | I/O | Host PC Data Bit 11 |
| 172 | HDRQ6 | RQ6 | OUT | Host PC Channel 6 DMA Request |
| 173 | HD10 | DHA | I/O | Host PC Data Bit 10 |
| 174 | HDACK6 | ACK6 | IN | Host PC Channel 6 DMA Acknowledge |
| 175 | HD9 | DH9 | I/O | Host PC Data Bit 9 |
| 176 | HDRQ5 | RQ5 | OUT | Host PC Channel 5 DMA Request |
| 177 | HD8 | DH8 | I/O | Host PC Data Bit 8 |
| 178 | HDHE* | DHEH | OUT | Host PC Data Bus High Byte Enable |
| 179 | HDACK5 | ACK5 | IN | Host PC Channel 5 DMA Acknowledge |
| 180 | HDRQ0 | RQ0 | OUT | Host PC Channel 0 DMA Request |
| 181 | HDACK0 | ACK0 | IN | Host PC Channel 0 DMA Acknowledge |
| 182 | GND | | PWR | |
| 183 | VCC | | PWR | |
| 184 | HBHE* | BHEH | IN | Host PC Bus High Enable |
| 185 | HIRQ3 | IH3 | I/O | Host PC Interrupt Request 3 |
| 186 | HIRQ2 | IH2 | I/O | Host PC Interrupt Request 2 |
| 187 | HIRQ1 | IH1 | I/O | Host PC Interrupt Request 1 |
| 188 | HIRQ0 | IH0 | I/O | Host PC Interrupt Request 0 |
| 189 | HA0 | AH0 | IN | Host PC Address Bit 0 |
| 190 | HA1 | AH1 | IN | Host PC Address Bit 1 |

| | | | | |
|---|---|---|---|---|
| 191 | HA2 | AH2 | IN | Host PC Address Bit 2 |
| 192 | HA3 | AH3 | IN | Host PC Address Bit 3 |
| 193 | HTC | TCH | IN | Host PC DMA Terminal Count |
| 194 | HA4 | AH4 | IN | Host PC Address Bit 4 |
| 195 | HA5 | AH5 | IN | Host PC Address Bit 5 |
| 196 | HA6 | AH6 | IN | Host PC Address Bit 6 |
| 197 | HA7 | AH7 | IN | Host PC Address Bit 7 |
| 198 | HA8 | AH8 | IN | Host PC Address Bit 8 |
| 199 | HA9 | AH9 | IN | Host PC Address Bit 9 |
| 200 | HDRQ1 | RQ1 | OUT | Host PC Channel 1 DMA Request |
| 201 | HDACK1 | ACK1 | IN | Host PC Channel 1 DMA Acknowledge |
| 202 | HDRQ3 | RQ3 | OUT | Host PC Channel 3 DMA Request |
| 203 | HDACK3 | ACK3 | IN | Host PC Channel 3 DMA Acknowledge |
| 204 | HIOR* | IORH | IN | Host PC I/O Read |
| 205 | HIOW* | IOWH | IN | Host PC I/O Write |
| 206 | HAEN* | AENH | IN | Host PC Address Enable |
| 207 | NC | | --- | |
| 208 | VCC | | PWR | |

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